REMARKS / ARGUMENTS

Status of Claims

Claims 1-23 are pending in the application and stand rejected. Of the pending claims, Applicant herein provides clarifying remarks, for consideration by the Examiner, to traverse the rejections. No claim amendments have been made, and therefore in compliance with 37 CFR 1.121, no claim listing is provided herewith.

Applicant respectfully submits that the rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) have been traversed, that no new matter has been entered, and that the application is in condition for allowance.

Rejections Under 35 U.S.C. §102

Regarding Examiner's paragraph 1, Applicant understands the Examiner's comment regarding the changes made to 35 U.S.C. §102(e) by the AIPA to be implying that the present application was not filed on or after November 29, 2000, when the record clearly shows that the present application was filed on March 20, 2002. Accordingly, Applicant invites the Examiner to provide clarifying comments as appropriate.

Regarding Examiner's paragraph 2, Claims 1, 9 and 16 stand rejected under 35 U.S.C. §102(b) as being anticipated by Saletta et al. (U.S. Patent No. 4,827,369, hereinafter Saletta) or Farrington (U.S. Patent No. 4,996,646, hereinafter Farrington). The Examiner alleges that Saletta discloses the claimed invention by referencing Figure 3, items 100, 82, 79, and 77a, and col. 3, lines 1-45. The Examiner further alleges that Farrington discloses the claimed invention by referencing col. 1, lines 40-70+ and col. 20, lines 45-70+. (Paper 3, page 3). Applicant traverses these rejections for the following reasons.

Saletta discloses a circuit interrupter arrangement for sampling a conditioned current value and determining operating characteristics related to the current flow through an electrical circuit. (Abstract). A trip unit 12 is used for selectively adjusting the tripping parameters under which the circuit interrupter is intended to operate. (Figure 3

and col. 4, lines 63-66). A microprocessor 100 controls the flow of data through the solid-state circuit interrupter 60. (Figure 3 and col. 10, lines 19-20). An A/D converter 82 communicates with microprocessor 100. (Figure 3 and col. 10, lines 34-39). A multi-purpose custom IC 79 includes a current multiplexing portion 79a that is controlled by signals from the microprocessor 100 so that a particular current signal may be selected and output from the multi-purpose custom IC 79 upon command of the microprocessor 100. (Figure 3 and col. 9, lines 57-65). A power supply 77, 77a regulates and converts a specific DC voltage output from a capacitor to a regulated DC voltage usable by the remaining circuitry of the solid-state circuit interrupter 60. (Figure 3 and col. 9, lines 16-23). The solid-state circuit interrupter 60 has an object of inexpensively and efficiently controlling the current through an electrical distribution circuit and providing such protections instantaneous, short delay, and long delay protection, while also providing the user with an ability to easily monitor the conditions under which these protections are being provided. (Col. 3, line 1-45).

Farrington discloses a network of microprocessor operated circuit breakers capable of communications with a central computer and with digital meters. (Figures 12-14 and 21-24, and col. 1, lines 40-61).

Notably absent from Saletta and Farrington is a power supply being configured to receive a first current, or a second current alone or in combination with the first current, the power supply providing an output to the microprocessor indicative of whether the power supply is receiving a second current, and the microprocessor being configured to adjust between the first and second states depending upon the output.

Applicant respectfully submits that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, ***in a single prior art reference***." *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (emphasis added). Moreover, "[t]he identical invention must be shown in as complete detail as is contained in the *** claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Furthermore, the single source must disclose all of the claimed elements

"arranged as in the claim." Structural Rubber Prods. Co. v. Park Rubber Co., 749 F.2d 707, 716, 223 U.S.P.Q. 1264, 1271 (Fed. Cir. 1984). Missing elements may not be supplied by the knowledge of one skilled in the art or the disclosure of another reference. Titanium Metals Corp. v. Banner, 778 F.2d 775, 780, 227 U.S.P.Q. 773, 777 (Fed. Cir. 1985).

In looking to Saletta to anticipate the instant invention, the Examiner references Figure 3, items 100, 79 and 77a, and col. 3, lines 1-45, alleging a microprocessor operable at either a first state or a second state, the second state requiring more power than the first state, in combination with a power supply being configured to receive a first current, or a second current alone or in combination with the first current, the power supply providing an output to the microprocessor indicative of whether the power supply is receiving a second current, and the microprocessor being configured to adjust between the first and second states depending upon the output.

In respectful disagreement with the Examiner, Applicant finds no such disclosure in Saletta. Specifically, Applicant finds Saletta to disclose a power supply 77, 77a that regulates and converts a specific DC voltage output from a capacitor to a regulated DC voltage usable by the remaining circuitry of the solid-state circuit interrupter 60. (Figure 3 and col. 9, lines 16-23), and not a power supply configured to receive a first current, *or a second current alone or in combination with the first current, the power supply providing an output to the microprocessor indicative of whether the power supply is receiving a second current*, as claimed in the instant invention. Also, Applicant finds Saletta to disclose a microprocessor 100 that controls the flow of data through the solid-state circuit interrupter 60 (Figure 3 and col. 10, lines 19-20), but not *a microprocessor being configured to adjust between a first and a second state depending upon the output of a power supply where the second state requires more power than the first state*, as claimed in the instant invention.

As an alternative to Saletta, the Examiner looks to Farrington to anticipate the instant invention by referencing Figures 12-14 and 21-24, col. 1, lines 40-70+, and col. 20, lines 45-70+. Here, the Examiner alleges that Farrington anticipates the claimed

invention by making a broad conclusory statement without specifically identifying how Farrington discloses each and every element of the claimed invention. Also, it is unclear what the Examiner's intent is by referring to lines 40-70+ and lines 45-70+, respectively, which Applicant understands to mean lines 40-68 and lines 45-69, respectively. In viewing Farrington as referenced by the Examiner and best understood by Applicant, Applicant finds Farrington to disclose a network of microprocessor operated circuit breakers capable of communications with a central computer and with digital meters. (Figures 12-14 and 21-24, and col. 1, lines 40-68). Regarding col. 20, lines 45-69, of Farrington, Applicant does not find the claimed invention disclosed at all, and the Examiner has not sufficiently explained how Farrington does disclose the claimed invention.

Dependent claims inherit all of the limitations of the respective parent claim.

In view of the foregoing remarks, Applicant submits that the References do not separately disclose each and every element of the claimed invention and therefore cannot be anticipatory, and that the Examiner has not properly met the burden of showing anticipation. Accordingly, Applicant respectfully submits and that the rejections under 35 U.S.C. §102(b) have been traversed, and requests that the Examiner reconsider and withdraw all of these rejections.

Rejections Under 35 U.S.C. §103(a)

Claims 1-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kornblit (U.S. Patent No. 6,473,281, hereinafter Kornblit) in combination with Saletta.

The Examiner alleges that Kornblit discloses at Figure 5 the claimed invention except that Kornblit does not disclose the utilization of the technique for auxiliary power supply. To cure this deficiency, the Examiner looks to Saletta at Figure 3, and alleges that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kornblit's trip unit by utilizing the technique taught by Saletta for the purpose of increasing the protection and reliability of the unit. (Paper 3, page 4).

Applicant traverses the Examiner's rejections for the following reasons.

Kornblit discloses a ground fault protection arrangement having sensors 31, 33, a trip module 40, and a trip unit 18. (Figure 5, and col.3, line 59 through col. 4, line 47). Kornblit is notably absent a power supply being configured to receive a first current, or a second current alone or in combination with the first current, the power supply providing an output to the microprocessor indicative of whether the power supply is receiving a second current, and the microprocessor being configured to adjust between the first and second states depending upon the output.

Applicant respectfully submits that the obviousness rejection based on the References is improper as the References fail to teach or suggest each and every element of the instant invention. For an obviousness rejection to be proper, the Examiner must meet the burden of establishing a prima facie case of obviousness. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). The Examiner must meet the burden of establishing that all elements of the invention are taught or suggested in the prior art. MPEP §2143.03.

The Examiner acknowledges that Kornblit does not disclose all elements of the claimed invention and looks to Saletta to cure this deficiency. However, as discussed previously and in reference to the rejections under 35 U.S.C. §102(b), Saletta does not cure the deficiency of Kornblit, and the combination of Kornblit and Saletta is specifically absent *a power supply being configured to receive a first current, or a second current alone or in combination with the first current, the power supply providing an output to the microprocessor indicative of whether the power supply is receiving a second current, and the microprocessor being configured to adjust between the first and second states depending upon the output*, as claimed in the instant invention.

In view of the foregoing, Applicant submits that the References fail to teach or suggest each and every element of the claimed invention and disclose substantially different inventions from the claimed invention, and therefore cannot properly be used to establish a prima facie case of obviousness. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Additionally, Applicant respectfully submits that an Examiner cannot establish obviousness by locating references which describe various aspects of a patent Applicant's invention without also providing evidence of the motivating force which would impel one skilled in the art to do what the patent Applicant has done. *Ex parte Levengood*, 28, USPQ2d 1300, 1302 (Bd.Pat.App.Int., 1993). References may not be combined indiscriminately. It is not enough for a valid rejection to view the prior art in retrospect once an Applicant's disclosure is known. The art applied should be viewed by itself to see if it fairly disclosed doing what an Applicant has done. *In re Skoll*, 187 USPQ 481, 484 (CCPA, 1975) (citing *In re Schaffer*, 108 USPQ 326, 328-29 (CCPA, 1956)). "The test for an implicit showing [of obviousness] is what the combined teachings, knowledge of one of ordinary skill in the art, and ***the nature of the problem to be solved as a whole*** would have suggested to those of ordinary skill in the art." (Emphasis added). *In re Kotzab*, 217 F.3d 13645, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

Saletta is generally concerned with a solid state circuit interrupter in molded case and metal clad type circuit interrupters that are capable of acting on a number of complex electrical parameters in order to protect the electrical conducting system and devices connected thereto, and that allow for system user interaction so that the number of electrical parameters can be easily and readily understood and responded to. (Co. 1, lines 25-35).

Kornblit is generally concerned with a need in the art for a circuit breaker implementing a ground-fault sensing circuit that annunciates a ground fault condition but does not open the power circuit in the case of a ground-fault condition. (Col. 1, lines 34-37).

Neither Saletta nor Kornblit, either singly or in combination, appear to be concerned with, or recognize the advantages of, *a power supply being configured to receive a first current, or a second current alone or in combination with the first current, the power supply providing an output to the microprocessor indicative of whether the power supply is receiving a second current, and the microprocessor being configured to*

adjust between the first and second states depending upon the output, as claimed in the instant invention.

At paragraph [0022] of the instant specification, Applicant discusses the microprocessor 28 being configured to adjust power consumption of the trip unit 10 on the fly, depending on the state of the second current 56 from the auxiliary power source 58. The microprocessor 28 continuously monitors the power supply 30 to determine whether the power supply is receiving the second current 56.

At paragraph [0027], Applicant discusses the microprocessor 28, running an algorithm 66, that operates at different clock speeds when operating in a first and a second state 70, 72, where the microprocessor runs faster at higher clock speeds and consumes proportionately more power.

At paragraph [0032], Applicant discusses the trip unit 10 optimizing the number of features and functions available according to the available power by adjusting the consumption of power.

Applicant finds Saletta and Kornblit to be absent any concern or recognition of the problem solved by the instant invention.

The Examiner alleges that one skilled in the art would have been motivated to modify Kornblit's trip unit by utilizing the technique taught by Saletta for the purpose of increasing the protection and reliability of the unit. However, since neither Saletta nor Kornblit teach or suggest signal communication between the power supply and the microprocessor for the purpose of enabling the microprocessor to adjust between a first state and a second state for optimizing power consumption, there can be no motivation to combine Saletta with Kornblit for this purpose. In arriving at an absence of any teaching to combine the References, one skilled in the art does not arrive at the claimed invention.

In view of the foregoing, Applicant submits that no motivation can be found in either of the References to combine the technologies of the References to arrive at the claimed invention, and that the Examiner has improperly combined the References since there is no evidence of a motivating force which would impel one skilled in the art to do

what the patent Applicant has done. Accordingly, Applicant respectfully requests reconsideration and withdrawal of all rejections under 35 U.S.C. §103(a).

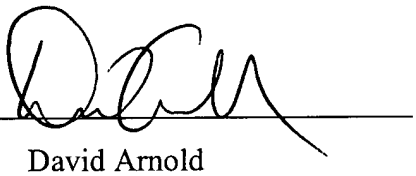
In light of the forgoing, Applicant respectfully submits that the Examiner's rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) have been traversed, and respectfully request that the Examiner reconsider and withdraw these rejections.

The Commissioner is hereby authorized to charge any additional fees that may be required for this amendment, or credit any overpayment, to Deposit Account No. 06-1130.

In the event that an extension of time is required, or may be required in addition to that requested in a petition for extension of time, the Commissioner is requested to grant a petition for that extension of time that is required to make this response timely and is hereby authorized to charge any fee for such an extension of time or credit any overpayment for an extension of time to the above identified Deposit Account.

Respectfully submitted,

CANTOR COLBURN LLP
Applicant's Attorneys

By: 

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